CLAIMS

1. A method of controlling a display device comprising an array of display pixels, each pixel comprising a thin film transistor switching device (14) and a display element (16), the array being arranged in rows and columns with each column of pixels sharing a column conductor (12) to which pixel data voltages are provided, the method comprising, for each field period (T_F) during which data is stored into the array of pixels:

providing a pixel drive signal to each pixel for storage on the pixel for a first period of time, the pixel drive signal comprising a selected one of a plurality of pixel drive levels;

providing a second drive voltage to each pixel for a second period of time, wherein the durations of the first and second periods of time are controlled to vary the pixel light output.

2. A method as claimed in claim 1, wherein the pixel drive signal is provided to each pixel by providing a first row pulse on a row conductor (10) timed with the application of a pixel data voltage on the column conductor (12).

3. A method as claimed in claim 2, wherein the second drive voltage is provided to each pixel by providing a second row pulse on a row conductor timed with the application of the second drive voltage on the column conductor.

4. A method as claimed in claim 3, wherein the durations of the first and second periods of time are controlled by selecting the timing of the second row pulse relatively to the first row pulse.

5. A method as claimed in any preceding claim, wherein each pixel is addressed with a first polarity in a first group of field periods and with a second opposite polarity in a second group of field periods.

6. A method as claimed in claim 5, wherein the second drive voltage comprises a fixed reference drive voltage (VR1, VR2), and wherein a first reference drive voltage (VR1) is provided for pixels driven to the first polarity and a second reference drive voltage (VR2) is provided for pixels driven to the second polarity.

7. A method as claimed in claim 6, wherein the first reference drive voltage (VR1) is of equal magnitude and opposite polarity to the second reference drive voltage (VR2).

8. A method as claimed in any preceding claim, wherein the durations of the first and second periods of time are together substantially equal to the field period (T_F).

9. A method as claimed in any one of claims 1 to 7, wherein the method further comprises providing zero volts to each pixel for a third period of time.

10. A method as claimed in claim 9, wherein the durations of the first, second and third periods of time are together substantially equal to the field period (T_F).

11. A method as claimed in claim 9 or 10, wherein providing zero volts to each pixel comprises resetting the pixel by discharging a pixel storage capacitor (20).

12. A method as claimed in any one of claims 9 to 11, wherein the method comprises controlling the durations of the first, second and third periods of time to vary the pixel light output.

13. A method as claimed in any one of claims 1 to 8, wherein each pixel comprises a pixel storage capacitor (20), and wherein the step of providing a pixel drive signal to each pixel for storage on the pixel for a first period of time

comprises applying a pixel data voltage to the column (12) and forming the pixel drive signal by capacitive coupling using the pixel storage capacitor (20).

14. A method as claimed in claim 1 or 2, wherein each pixel comprises a pixel storage capacitor (20), and wherein the step of providing a second drive voltage to each pixel for a second period of time comprises modifying the pixel drive signal to form the second drive voltage by capacitive coupling using the pixel storage capacitor.

15. A method as claimed in claim 14, wherein the step of modifying the pixel drive signal by capacitive coupling comprises applying a voltage waveform (Capacitor) to one terminal of the pixel capacitors (20) for each row of pixels.

16. A method as claimed in claim 15, wherein the voltage waveform (Capacitor) has two levels 9VC1, VC2), and the timing of the transitions between the two levels determines the durations of the first and second periods of time.

17. A method as claimed in claim 15, wherein the voltage waveform (Capacitor) has three levels (VC1, 0, VC2), and the timing of the transitions between the three levels determines the durations of the first and second periods of time.

18. A method as claimed in any one of claims 14 to 17, wherein each pixel is addressed with a first polarity in a first group of field periods and with a second opposite polarity in a second group of field periods.

19. A method as claimed in any preceding claim, wherein the plurality of pixel drive levels correspond to a 4, 6, 8 or 10 bit pixel drive signal.

20. A method as claimed in any preceding claim, wherein the second period of time can be varied between a duration of 0 and at least 0.5 times the field period.

21. A method as claimed in any preceding claim, wherein the display pixels comprises twisted nematic liquid crystal display pixels.

22. A method as claimed in any preceding claim, wherein the second drive voltage corresponds to a drive level for the pixel which is between the brightest and darkest pixel drive levels.

23. A display device comprising an array of display pixels, each pixel comprising a thin film transistor switching device (14) and a display element (16), the array being arranged in rows and columns with each column of pixels sharing a column conductor (12) to which pixel drive signals are provided, wherein the device comprises column driver circuitry (32) for generating analogue pixel drive signals, the column driver circuitry (32) further comprising means for generating at least one reference drive voltage (VR1, VR2), and wherein the device further comprises timing means for controlling the duration of application of pixel drive signals and of the reference drive voltage to the display pixels.

24. A device as claimed in claim 23, wherein the column driver circuitry comprising means for generating two reference drive voltages (VR1, VR2) of equal magnitude and opposite polarity.